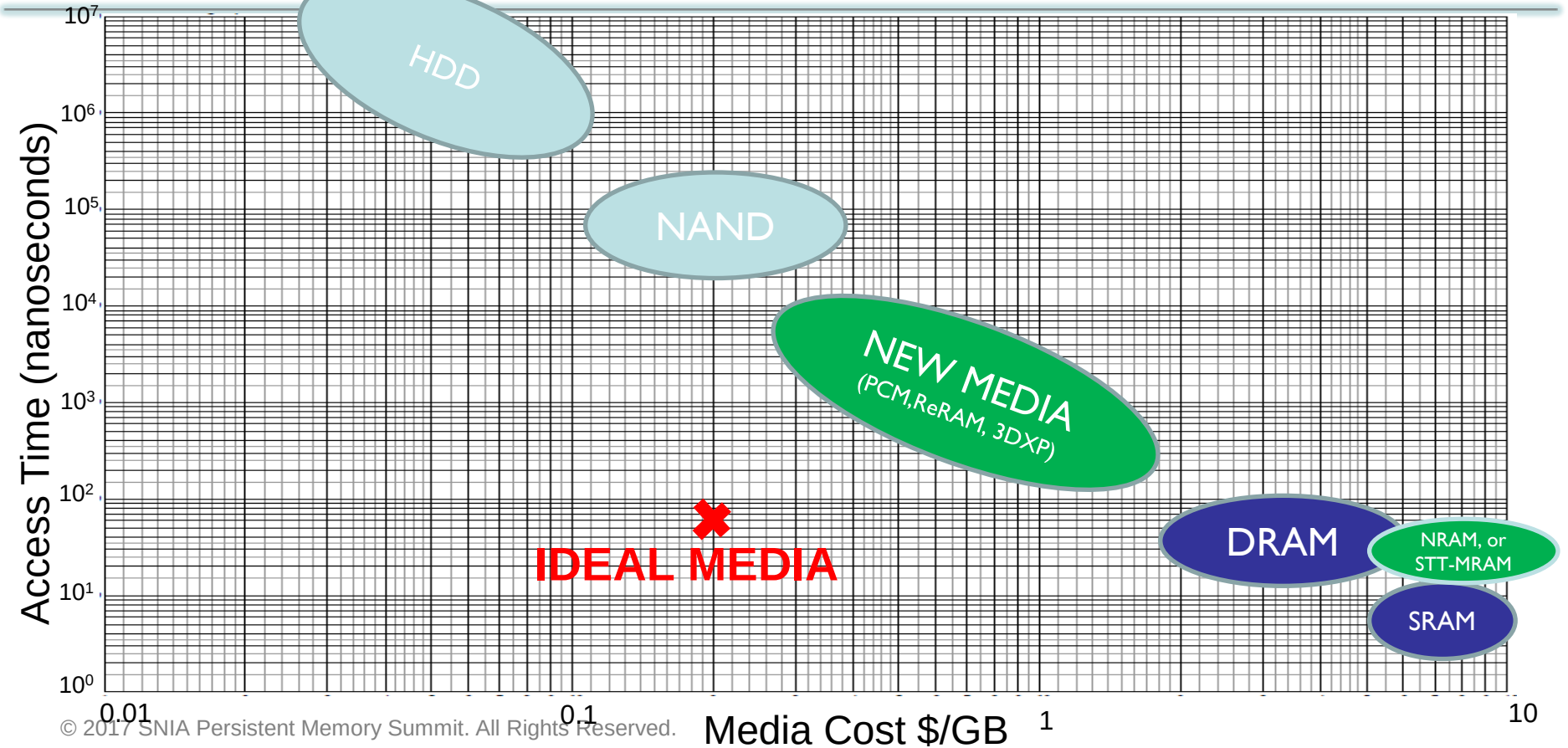
Next Generation Persistent Memory Evolution beyond the NVDIMM-N

Doug Finke, Xitore, Inc.

NVDIMM-P can make current DRAM/NAND Competitive with more Exotic New Media



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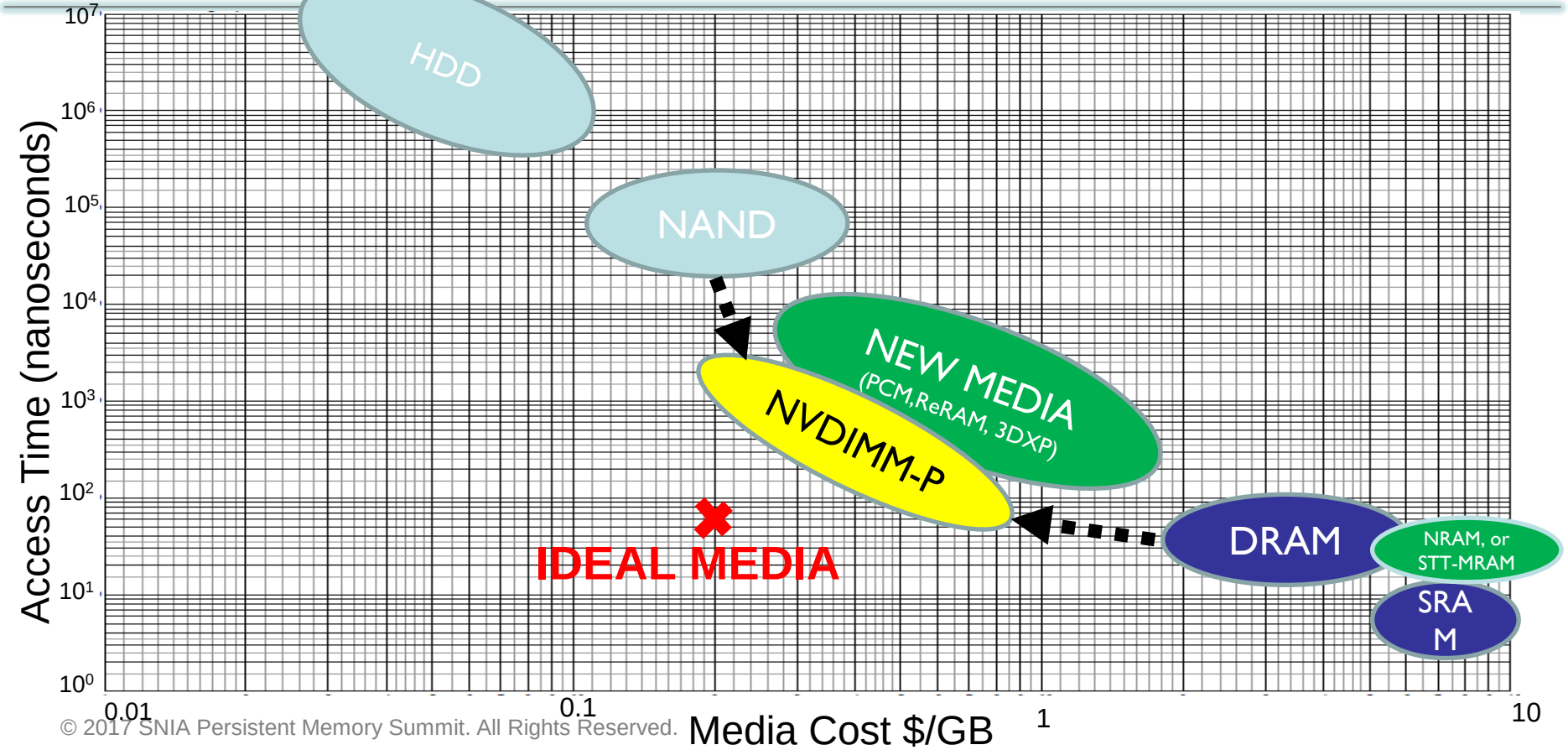
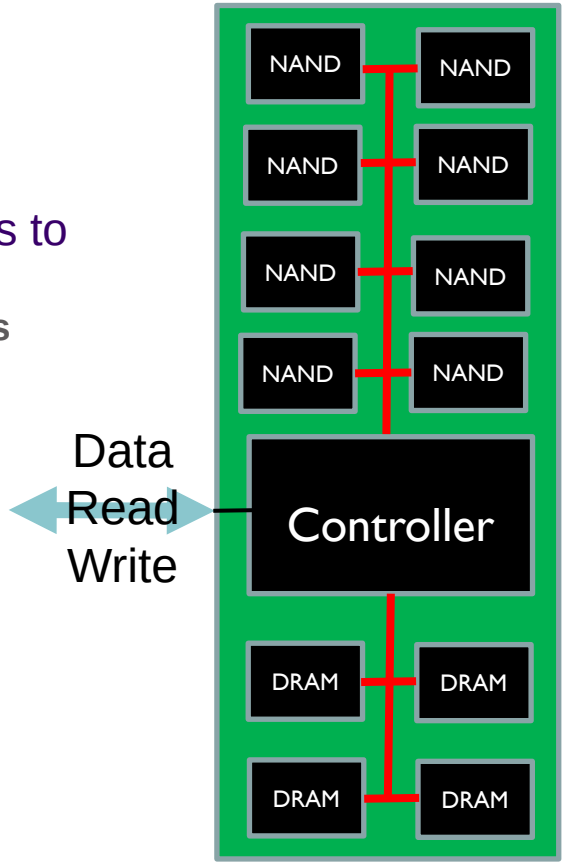


Key Elements of a Cache-Based NVDIMM Architecture

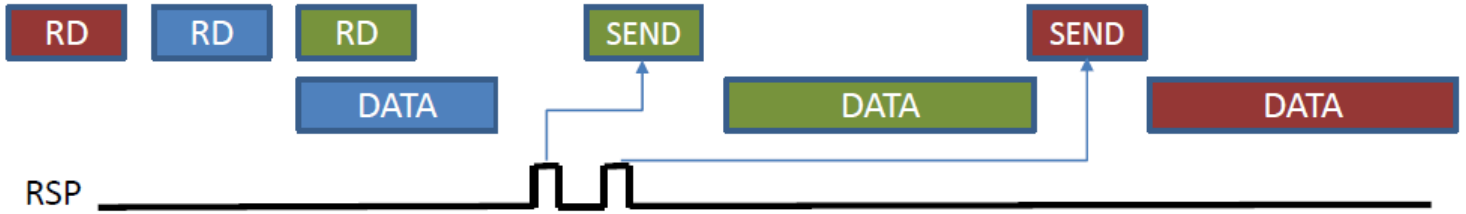
- NVDIMM-N is a shadow memory based architecture
  - DRAM and NAND size are about the same and cover the same address space
- NVDIMM-P is a protocol to allow non-deterministic accesses to enable a cache-based NVDIMM architecture
  - DRAM size is a fraction of the NAND size; **Significant cost advantages**
- Tiered, heterogeneous memory on the same DIMM
  - Both fast and slow memory connected in a cache architecture
- Private on-DIMM memory bus between the fast and slow memories
  - Doesn't tie up the main memory bus for line fetches and cast-outs
- Implement a command queuing capability like HDDs
  - Helps hide latencies when there is a cache miss



Challenge – Deterministic DRAM Bus

Potential Solutions

- Industry working on adding new control pins and associated protocol to a DDR4 extension and the standard DDR5 busses to handle variable access times



- Use a special driver and programming of the CPU page table
- Provide a backwards compatibility mode and driver to work on existing systems in a block mode

Implications for New Media

- Large scale adoption of new media technology will be slowed due to the onset of cache-based NVDIMMs
- Impact will raise the bar for the new technologies and they will require forcing further cost reductions
  - Published reports of costs/bit are roughly 50% of DRAM, but 500% that of NAND
  - Will need to achieve costs structure closer to NAND before going mainstream
- Once costs get closer to those of NAND the same cache-based NVDIMM concepts will be used by replacing the NAND/DRAM with the appropriate new technology

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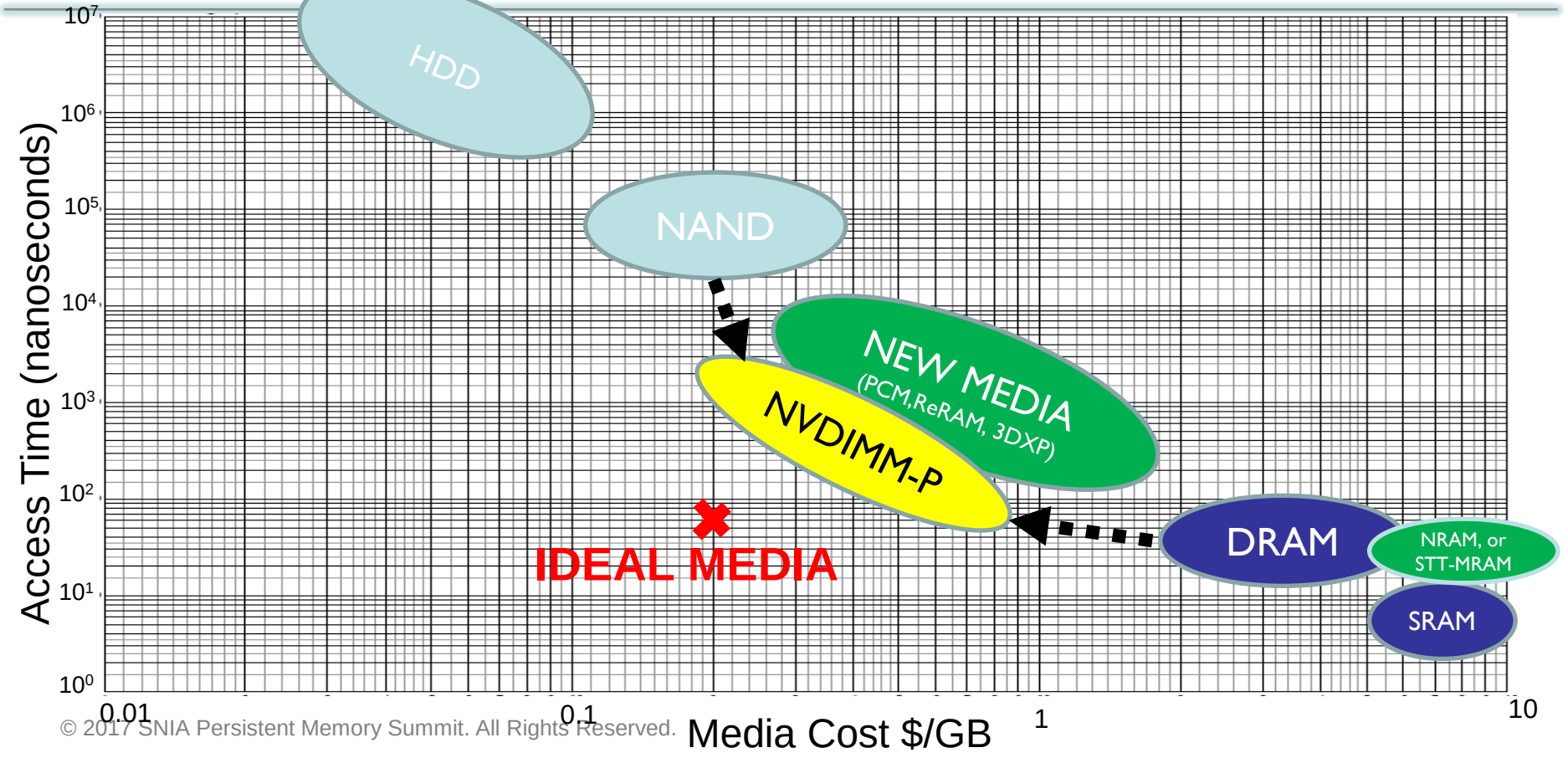
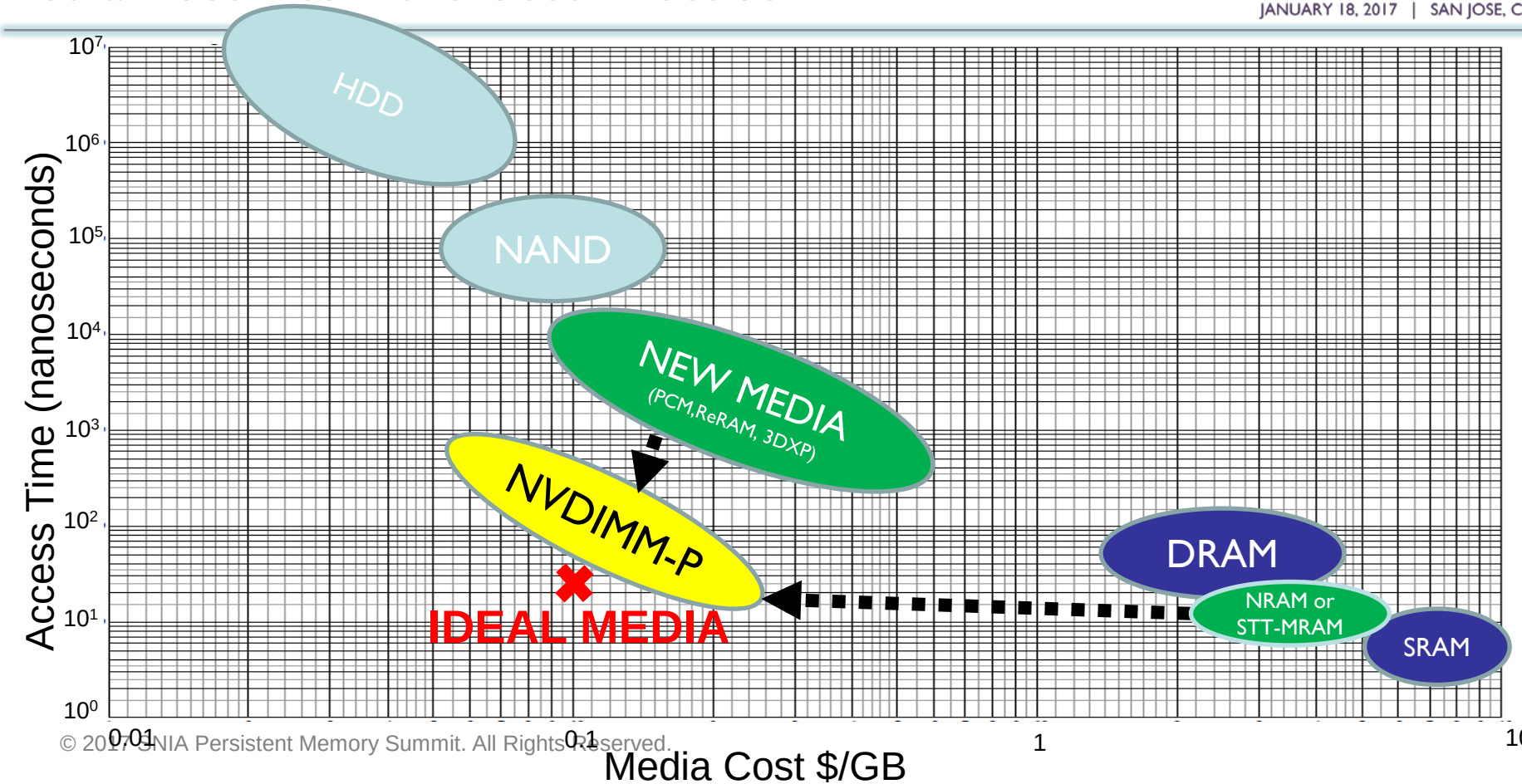


Use Same NVDIMM-P Architecture when the New Media Becomes More Cost Effective



Conclusion – Persistent Memory in the 2020's

- Enterprise SSD interfaces will always migrate to the fastest bus available
  - NVMe → DDR4 → DDR5 → GenZ or OpenCapi
- Byte mode (or DAX) access will be heavily adopted and provide further performance improvements
- On-module cache-based architectures with fast and slow memories will become the standard
  - DRAM/NAND initially, with potential new media replacements later on
- Command queuing, not used with DRAMs today, will become a standard
  - Enables execution out-of-order when latencies are variable
  - Will help to hide latencies associated with cache misses
- **Cache-based NVDIMM architectures will be the predominant interface overtaking NVMe within the next 5-10 years in the race for performance**

NVDIMM **NVMe**