Xitore, Inc.

Comparison of the NVDIMM-X with 3D Xpoint in a DIMM Form Factor

Doug Finke
Director of Product Marketing
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Intel is expected to release a version of the 3D Xpoint technology in a DIMM form factor in 2018. Although many details regarding this technology are still not known there is some information that has been released. From the available information, we have observed a number of possible drawbacks that will position Xitore's NVDIMM-X favorably compared with 3D Xpoint DIMM. These are described below.

NVDIMM-X Has a Significant Cost Advantage over 3D Xpoint DIMM

The 3D Xpoint non-volatile memory media solution is positioned as a technology that is in-between that of DRAM and NAND. Specifically, it is touted to have a cost of about one-half that of DRAM, but still 5X that of NAND. This is due to that the fact that the manufacturing process requires over 100 new materials, significant investments in new manufacturing equipment and process, manufacturing yield challenges (as with any new process/technology) and lower throughput in the wafer fab than a normal semiconductor device. All of these factors will increase the manufacturing cost of 3D Xpoint non-volatile memory media.

Contrast that to the NVDIMM-X, which uses commodity DRAM and NAND chips that have been production optimized for over 30 years. Cost reductions will continue as conversion of NAND to 3D NAND technology proceeds. Although the NVDIMM-X will use some DRAM it represents only a small fraction of the total memory on the DIMM module. Most of the memory cost will be in the low cost NAND chips, so the NVDIMM-X should have a significant cost advantage over 3D Xpoint DIMM solutions.

To show more explicitly how significant this difference is, the table below compares solely the media costs in both technologies for a 1TB storage of a single NVDIMM module that contains 8GB or 16GB of DRAM cache. These numbers are based upon current pricing published by the DRAM Exchange and statements from Intel and Micron of the 3D Xpoint media costs versus DRAM devices.

Media Type	**3D Xpoint DIMM**	**NVDIMM-X**
DRAM – 8GB or 16GB	$22 (8GB)	$44 (16GB)
MLC NAND - 1024GB	$0	$512
3DXP Chips - 1024GB	$2816	$0
Total	**$2838**	**$556**

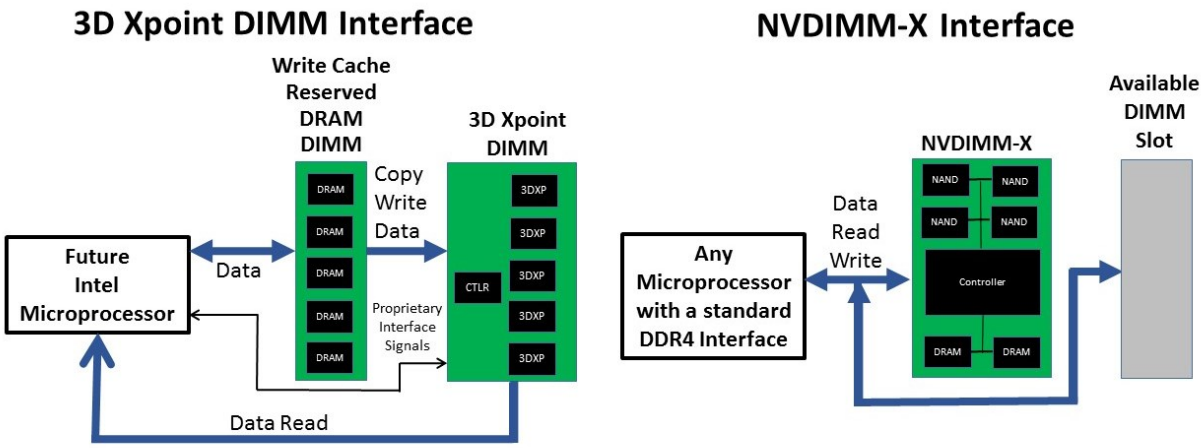
Note: These costs are media costs only and do not include any additional costs associated with the controller, PCB, other minor components, or test and assembly costs.

NVDIMM-X is Expected to Have Similar or Better Latencies and Bandwidth to that of 3D Xpoint DIMM

Since the NVDIMM-X uses a cache architecture, most of the accesses will utilize the on-board DRAM cache so that the effective latencies will be similar to DRAM latencies. Although there will be some accesses that will be a "cache miss" and require fetching the data from the lower speed NAND, algorithms within the NVDIMM-X control logic will minimize this so that the "cache hit" ratio remains at a high level and effective latencies remain very promising. In addition, the NVDIMM-X supports a 128 entry command queue. So when there is a cache miss and a piece of data needs to be fetched from the NAND, the NVDIMM-X can still process other commands while waiting for the NAND transfer to complete. This internal parallelism can significantly improve overall system throughput versus those architectures which can only process one or two commands at a time.

NVDIMM-X Cache Architecture Provides Improved DRAM Bus Efficiency

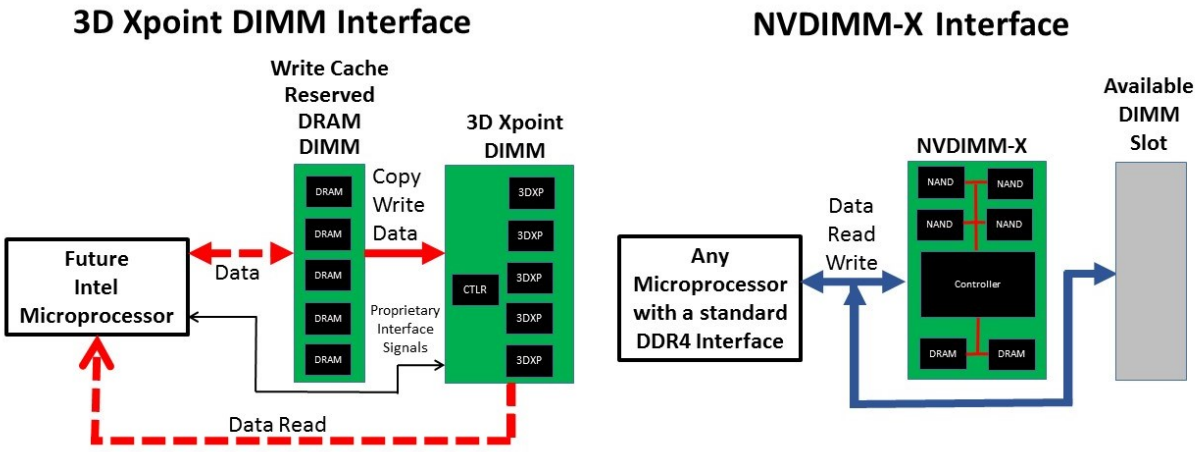
Although both the NVDIMM-X and 3D Xpoint DIMM uses DRAM as their cache memories, there is a big difference because the NVIDMM-X uses an "on-board" cache versus the 3D Xpoint DIMM, which uses a separate standard DRAM DIMM module for the cache. The 3D Xpoint DIMM uses external separate standard DRAM DIMM module as a write cache architecture and is required because the write accesses are much slower than the read accesses in 3D Xpoint media. The interface diagram below compares the connection topology of the 3D Xpoint DIMM versus the NVDIMM-X.



Note that every 3D Xpoint usage will consume two DIMM slots in the system. The NVDIMM-X will only use one.

The 3D Xpoint DIMM architecture has two disadvantages. First, since every 3D Xpoint DIMM requires another external separate DRAM DIMM module to function, it requires twice the number of DIMM slots to operate. Second, it will utilize bus bandwidth when the system is required to transfer data from the external separate DRAM cache DIMM module back to the 3D Xpoint DIMM. These transfers are controlled by the memory management unit in the microprocessor and during these transfers the DRAM bus is not available for a different access to another DIMM on this same channel until the cache transfer is complete.

Because the NDIMM-X has the DRAM cache and NAND on the same module, the transfers back and forth to the cache are implemented on a private bus on the NVDIMM-X module. Because of this the main DRAM bus can be used at the same time for other transfers. This parallelism will improve performance and is shown below.



Bus availability during a write-back operation. Red denotes a bus that would not be available during this operation while blue represents a bus that would be available for other transactions during this time. (Note: The three red busses on the left are physically the same bus, but they are shown separately to better clarify how the data flows.)

The 3D Xpoint DIMM May Only Be Able to Support Specific Future Intel Microprocessors

Intel has disclosed that the 3D Xpoint DIMM will require some additional proprietary control signals that are not part of the JEDEC defined standard DDR4 bus. Per the interface diagrams above, it appears that these additional, proprietary signals will be implemented on a future Intel Xeon processor. This could have significant implications. First, it would mean that the 3D Xpoint DIMM would not work with any other manufacturer's processor, including AMD, ARM, SPARC, and others. In fact, it probably wouldn't even work with Intel's current generation of processor. Intel is adding some new processor instructions called CLWB, CLFLUSHOPT, and PCOMMIT to properly handle data persistency, which will only be available in the newer microprocessors. Second, unless Intel publicizes and licenses this interface, it would limit the supplier base for this technology to Intel only. In contrast, the NVDIMM-X will run on any microprocessor that supports the standard DDR4 bus and will not require any proprietary bus extensions or new instruction sets.

Summary

There is still a lot that isn't known about 3D Xpoint technology and there is evidence of both changes in schedule and possible changes in product direction as the development proceeds. As data is released, we will be able to provide more specifics regarding how Xitore's NVDIMM-X favorably compares to 3D Xpoint DIMM solutions.

We do expect that the first NVMe product using 3D Xpoint media will be released in a few months. These will still be subject to the performance limits inherent in the NVMe bus. The 3D Xpoint DIMMs are expected to be released much later in perhaps late 2017 or 2018 in conjunction with a new Intel microprocessor. We expect that Xitore's NVDIMM-X to compare very favorably to it. Bottom line, the NVDIMM-X should offer similar performance at a much reduced cost without requiring any proprietary changes to the JEDEC standard DDR4 bus.

However, long term there still may be a place for 3D Xpoint media if Intel can get its cost structure more in line to that of NAND. A future version of the NVDIMM-X could be built using 3D Xpoint media technology in place of the NAND currently that is currently being used. This could provide a further improvement in performance when there is a cache miss.

While the discussion in this white paper was oriented towards the 3D X-point technology, many of these points are also valid for other new media including ReRAM, PCM, MRAM, ST-RAM, and Memristor. When the new media technologies become mature enough to replace the NAND, the NVDIMM-X architecture will be the most logical interface to use. Since most of these new media technologies are faster than NAND but slower than DRAM, it would still make sense to utilize the NVDIMM-X architecture so that it can provide for the on-module DRAM cache. We look forward to further developments of these technologies and intend to integrate them into future products as they become cost-effective.

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